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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,971	02/13/2004	Naokazu Kuzuno	248965US2S	7450

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EXAMINER	
BAUER, SCOTT ALLEN	

ART UNIT	PAPER NUMBER
2836	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/777,971	KUZUNO ET AL.
	Examiner	Art Unit
	Scott Bauer	2836

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/13/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1,2 &7-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (US 5929691) in view of Kim et al. (US 6150868) and further in view of Verwegen (US 6147546). Note that for the purpose of this office action, Kim et al. (US 5929691) will be referred to as "*Kim et al.*" and Kim et al. (US 6252422) will be referred to as "*Kim et al. (US 6252422)*".

3. With regard to Claim 1, Kim et al., in Figure 7, teaches a fuse latch circuit comprising: a fuse (31); a first inverter (35), and first, second and third transistors (33, 36 & 34 respectively). The source of the first transistor (33) is coupled to a first power supply potential (Vdd), a drain is connected to the input of the inverter, and a pulse signal for initialization (ØC) is input to a gate. The source of the second transistor (36) is coupled to the first power supply potential (Vdd), the drain is connected the input end of the inverter, and a gate is connected to the output end of the first inverter; The source of the third transistor (34) is coupled to one end of the fuse, a drain is connected to the input of the inverter, and the pulse signal (ØC) is input to a gate. The second end of the fuse is connected to a second power supply potential. Kim et al. further teaches that the

fuse latch is placed between the source of the third transistor and the second power supply terminal, rather then being coupled between the input of the first inverter and the drain of the third transistor.

Kim et al. does not teach that a second inverter is connected to the output of the first inverter, or that the conductance of the first transistor is higher than that of the second transistor.

Kim et al. (US 6150868), in Figure 1, teaches an anti-fuse programming circuit wherein a second inverter is coupled to the output of a first inverter and the gate of a second transistor. Kim et al (US 6150868) further teaches that the fuse (70) is located at the drain of an NFET and is also coupled to the input of a first inverter and the drains of a first and a second PFET transistor.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Kim et al. with Kim et al. (US 6150868) by coupling a second inverter to the output of the first inverter, and placing the fuse at the drain of the NFET for the purpose of providing a non-inverted output with respect to the signal ØC.

Verwegen teaches a zero volt/current fuse arrangement wherein a fuse (2) is coupled to the drains of a PFET (6) and NFET (7) transistor. The source of the PFET is coupled to a first power supply terminal (Vdd) and the source of the NFET is connected to a second power supply terminal. Verwegen further states that the PFET (6) has a large W/L ratio and that the NFET (7) has a small W/L ratio (column 3 lines 41-56).

Thus causing the conductance of the first transistor to be higher then the conductance of the second transistor as the conductance is proportional to the transistor's W/L ratio.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Kim et al. in view of Kim et al. (US 6150868) with Verwegen, by selecting the sizes of the first and second transistors so that the first transistor has a higher conductance than that of the second transistor as taught by Verwegen, for the purpose of insuring that the voltage at the input of the inverter (35) is stable enough to be read as a logical "1" or a logical "0" (Verwegen column 3 lines 52-56).

4. With regard to Claim 2, Kim et al. in view of Kim et al. (US 6150868) and further in view of Verwegen discloses the fuse latch circuit of Claim 1. Kim et al. (US 6150868) further discloses that a circuit threshold value of the first inverter (INV1) is set to a half value of a total value of the first power supply potential and the second power supply potential (HVCC).

5. With regard to Claim 7, Kim et al. in view of Kim et al. (US 6150868) and further in view of Verwegen, discloses the fuse latch circuit of Claim 1. Kim et al. (US 6150868) further discloses that the third transistor (20) is formed immediately below the end portion of the fuse (70).

6. With regard to Claim 8, Kim et al. in view of Kim et al. (US 6150868) and further in view of Verwegen, discloses the fuse latch circuit of Claim 1. Kim et al. (US 6150868) further discloses that the fuse latch circuit is used for a redundancy circuit of memory (column 1 lines 16-18).

7. With regard to Claim 9, Kim et al. in view of Kim et al. (US 6150868) and further in view of Verwegen, discloses the fuse latch of Claim 1. Verwegen further discloses that the fuse can be an aluminum fuse (column 1 lines 44-49).

8. With regard to Claim 10, Kim et al. in view of Kim et al. (US 6150868) and further in view of Verwegen, discloses the fuse latch of Claim 1. Kim et al. further discloses that the fuse can be an electrical fuse (column 1 lines 29-32).

9. With regard to Claim 11, Kim et al. in view of Kim et al. (US 6150868) and further in view of Verwegen, discloses the fuse latch of Claim 1. Kim et al., in Figure 7, further discloses that the first transistor and second transistor are each a p-channel MOS transistor.

10. With regard to Claim 12, Kim et al. in view of Kim et al. (US 6150868) and further in view of Verwegen, discloses the fuse latch of Claim 1. Kim et al., in Figure 7, further discloses that the third transistor is an n-channel MOS transistor.

11. With regard to Claim 13, Kim et al. in view of Kim et al. (US 6150868) and further in view of Verwegen, discloses the fuse latch of Claim 1. Kim et al., in Figure 7, further discloses that the second power supply potential is a ground potential.

12. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. in view of Kim et al. (US 6150868) and further in view of view of Verwegen, as applied to Claim 1 above, and further in view of Saito et al. (US 6320800).

13. With regard to Claim 3, Kim et al. in view of Kim et al. (US 6150868) and further in view of Verwegen, discloses the fuse latch circuit according to Claim 1.

Kim et al. in view of Kim et al. (US 6150868) and further in view of Verwegen, does not teach that a plurality of fuse latch circuits form a fuse latch circuit group and that an internal circuit receives output signals of the fuse latch group.

Saito et al., in Figure 1, teaches a semiconductor memory having redundant circuitry comprising: a fuse circuit group (201) comprised of a plurality fuse circuits; and an internal circuit (101) which receives output signals of the fuse latch circuit group.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Kim et al. in view of Kim et al. (US 6150868) and further in view of Verwegen, with Saito et al., by placing the fuse latch circuit taught by Kim et al. in view of Kim et al. (US 6150868) and further in view of Verwegen, in the redundant column cell array fuse circuit (201) taught by Saito et al., for the purpose of using the fuse latch of Kim et al. in view of Kim et al. (US 6150868) and

further in view of Verwegen, to replace a defective cell in a memory cell array, thereby providing a faster method of memory read/write operations for an entire array of memory.

Further, Kim et al. in view of Kim et al. (US 6150868) and further in view of Verwegen, discloses the claimed invention of Claim 3 except that the fuse latch of Claim 1 is not arranged into a fuse latch group. It would have been obvious to one having ordinary skill in the art at the time the invention was made to arrange the fuse latch taught by Kim et al. in view of Kim et al. (US 6150868) and further in view of Verwegen, into a group of many fuse latch circuits, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. St. Regis Paper Co. v. Bemis Co., 193 USPQ 8.

14. Claims 4-6 & 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. in view of Kim et al. (US 6150868) and further in view of Verwegen, and Saito et al. as applied to Claim 1 above, and further in view of Kang (US 6134177).

15. With regard to Claim 4, Kim et al. in view of Kim et al. (US 6150868) and further in view of Verwegen, and Saito et al. teaches a semiconductor integrated circuit comprising: a plurality of fuse latch circuit groups each comprised of a plurality of fuse latch circuits; and an internal circuit which receives output signals of said plurality of fuse latch circuit groups, wherein each of said plurality of fuse latch circuits is the fuse

latch circuit according to Claim 1, and the pulse signals according to claim 1 are individually fed with different timings into said plurality of fuse latch circuit groups.

Kim et al. in view of Kim et al. (US 6150868) and further in view of Verwegen, and Saito et al. does not teach that pulse signals are individually fed with different timings into the plurality of fuse latch circuit groups.

Kang, in Figure 4, teaches a redundancy decoding circuit wherein the pulses to the fuse latch circuits (10) are individually fed with different timings into a plurality of fuse latch circuit groups (column 4 lines 13-25).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings Kim et al. in view of Kim et al. (US 6150868) and further in view of Verwegen, and Saito et al. with Kang, by driving the fuse latch circuit groups taught by Kim et al. in view of Kim et al. (US 6150868) and further in view of Verwegen, and Saito et al. with the pulse generator (20) taught by Kang, by driving each fuse latch circuit group with a different flip-flop output (Q0-Q3) for the purpose of reducing standby current during read/write operations (Kang column 4 lines 9-12).

16. With regard to Claims 5 & 6, Kim et al. in view of Kim et al. (US 6150868) and Verwegen, and further in view Saito et al and Kang discloses the semiconductor integrated circuit according to Claim 4. Kang, in Fig. 5, further teaches that the pulse signals (Q0-Q3) to be individually input to said plurality of fuse latch circuit groups, do not overlap timewise with one another (normal read/write mode). Kang further teaches

that the timings with which the pulse signals according to claim 1 are individually fed into said plurality of fuse latch circuit groups are controlled by a delay circuit (20) having a delay time longer than at least a width of the pulse signal, as demonstrated in Figure 5.

17. With regard to Claim 14, Kim et al. in view of Kim et al. (US 6150868) and Verwegen, and further in view Saito et al and Kang discloses the fuse latch of Claims 1, 3 & 4. Saito et al., in figure 5, further discloses that the output signal of fuse latch circuit group (201) is fed into an internal circuit via a bus (306) (column 10 lines 9-14).

18. With regard to Claim 15-17, Kim et al. in view of Kim et al. (US 6150868) and Verwegen, and further in view Saito et al and Kang discloses the fuse latch of Claims 1, 3 & 4. Saito et al., in figure 5, further discloses that fuse latch circuit is part of a memory.

19. Claims 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. in view of Kim et al. (US 6150868) and Verwegen, and further in view Saito et al and Kang as applied to claims 1, 3 & 4 above, and further in view of Potter et al. (US 6308230).

20. With regard to Claims 18-20, Kim et al. in view of Kim et al. (US 6150868) and Verwegen, and further in view Saito et al and Kang teaches the fuse latch element of

Claims 1, 3 & 4 wherein the fuse latch is part of a semiconductor integrated circuit memory.

Kim et al. in view of Kim et al. (US 6150868) and Verwegen and further in view Saito et al and Kang does not teach that the memory is in a memory embedded microcomputer.

Potter et al., teaches that a memory array can be embedded in a microcomputer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Kim et al. in view of Kim et al. (US 6150868) and Verwegen and further in view Saito et al and Kang with Potter et al., by placing the memory taught Kim et al. in view of Kim et al. (US 6150868) and Verwegen and further in view Saito et al and Kang, in the memory embedded microcomputer taught by Potter et al., for the purpose of saving cost and space on a circuit board by integrating two separate semiconductor integrated circuits into one integrated circuit.

Conclusion

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Bauer whose telephone number is 571-272-5986. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2058. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAB

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PRIMARY EXAMINER